FIG. 1

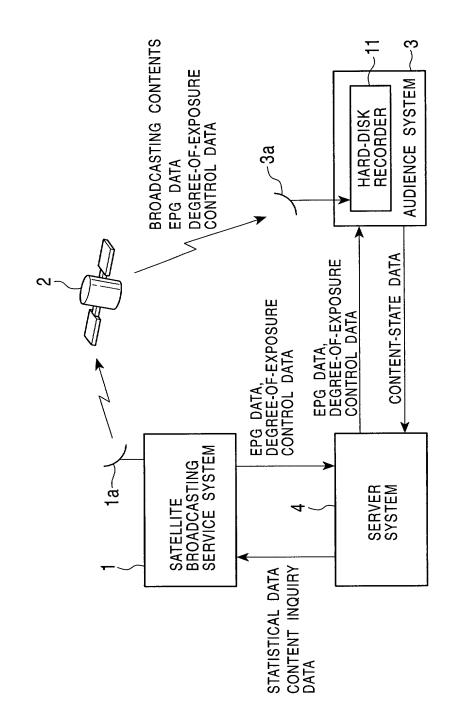
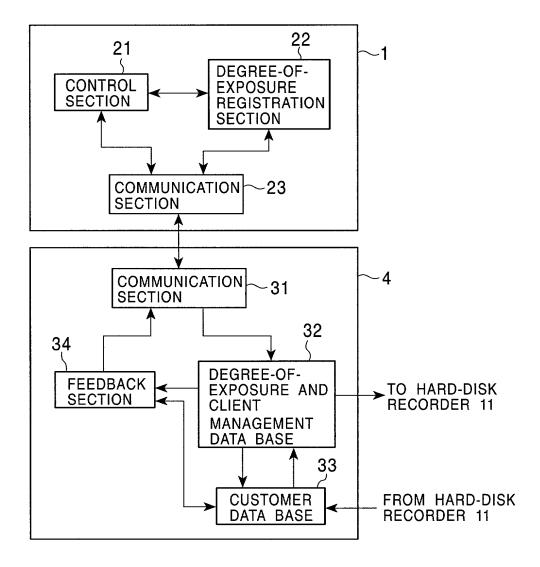
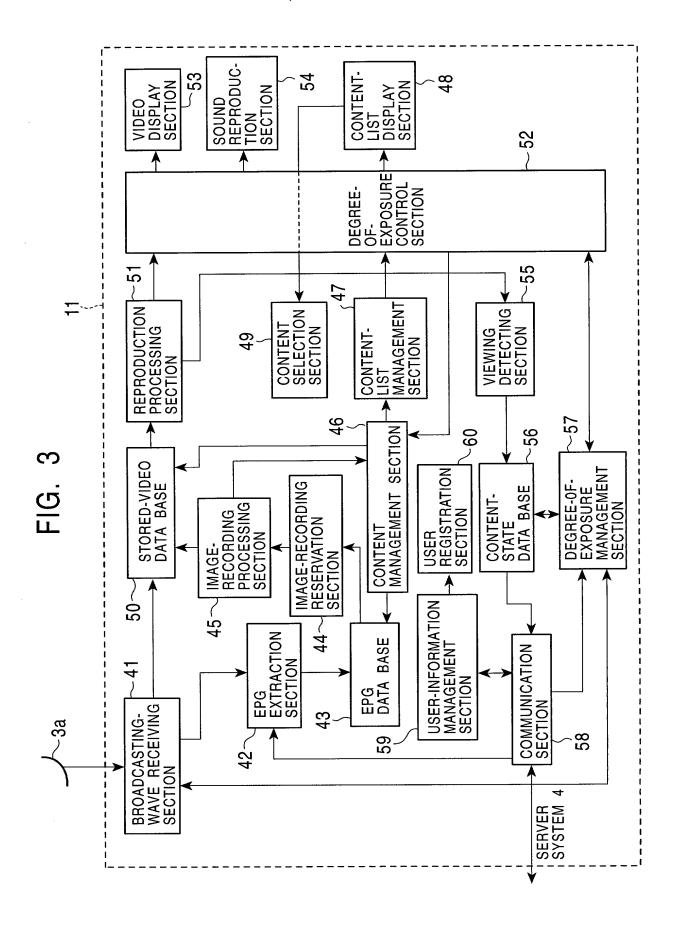


FIG. 2





DISPLAY 94 င်္ဂ 75 MUX 98 ~85 73 COMPOSER 모 HDD I/F -84a DECODER VIDEO CAMERA RAM IEEE1394 I/F 84 2 92~ ROM DEMODULATOR 83 BUS GRAPHIC PROCESSING CONTROLLER 85 7,2 RAM~ 80 <u>~</u> 78 COMMUNICATION CONTROL SECTION TUNER CPU U/I CONTROL SECTION BROADCASTING CONTENTS --76a 9

FIG. 4

FIG. 5A

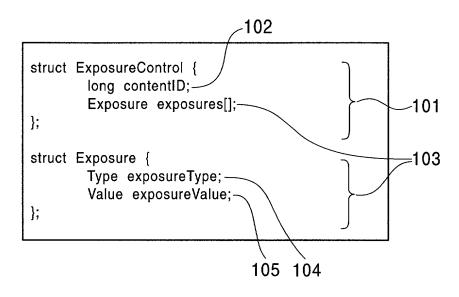
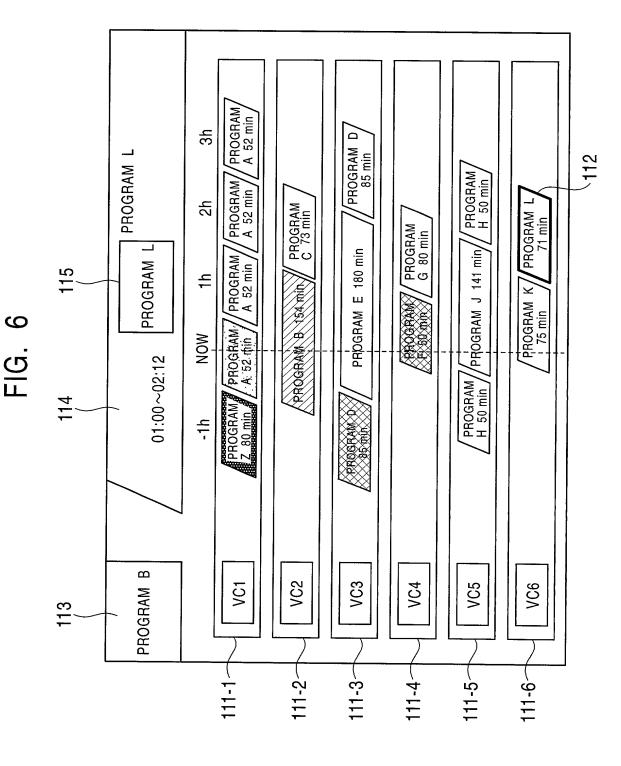
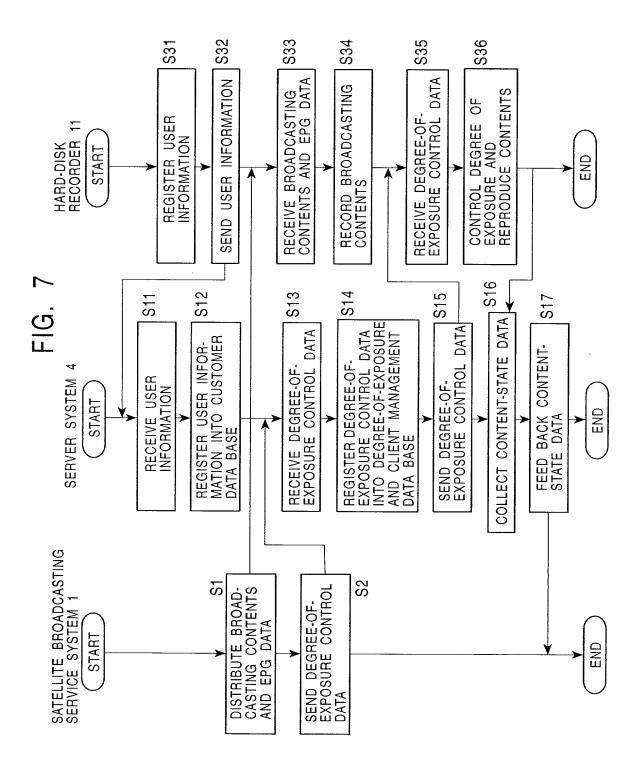
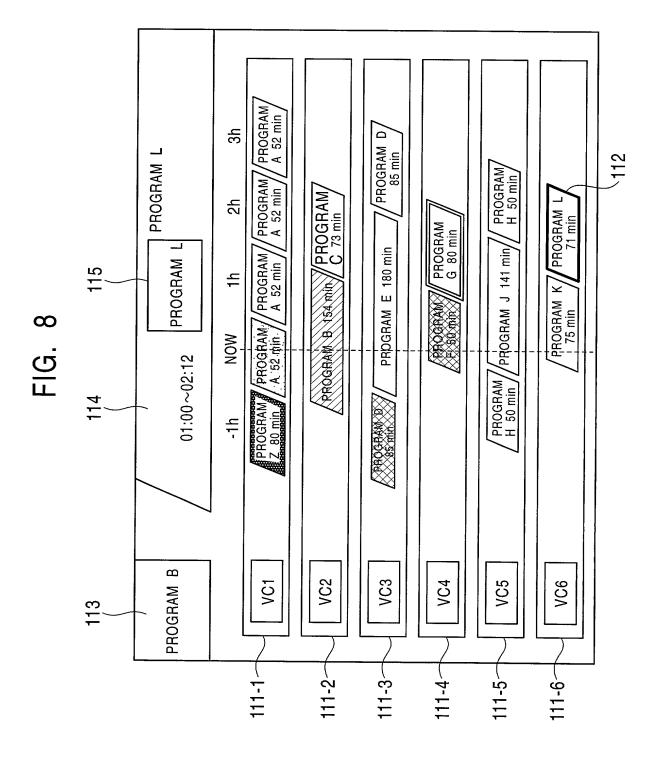
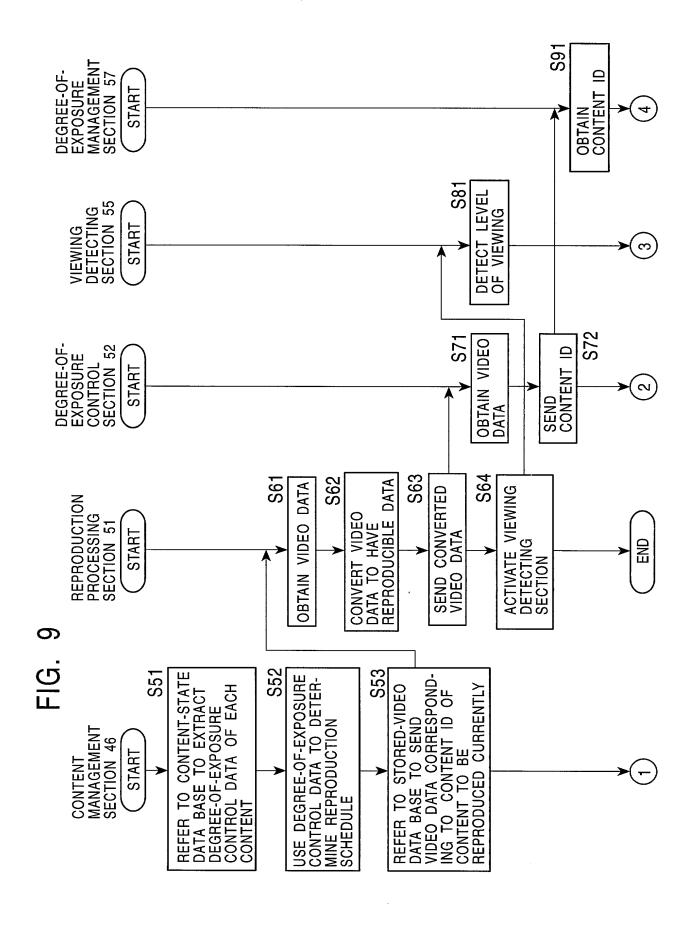


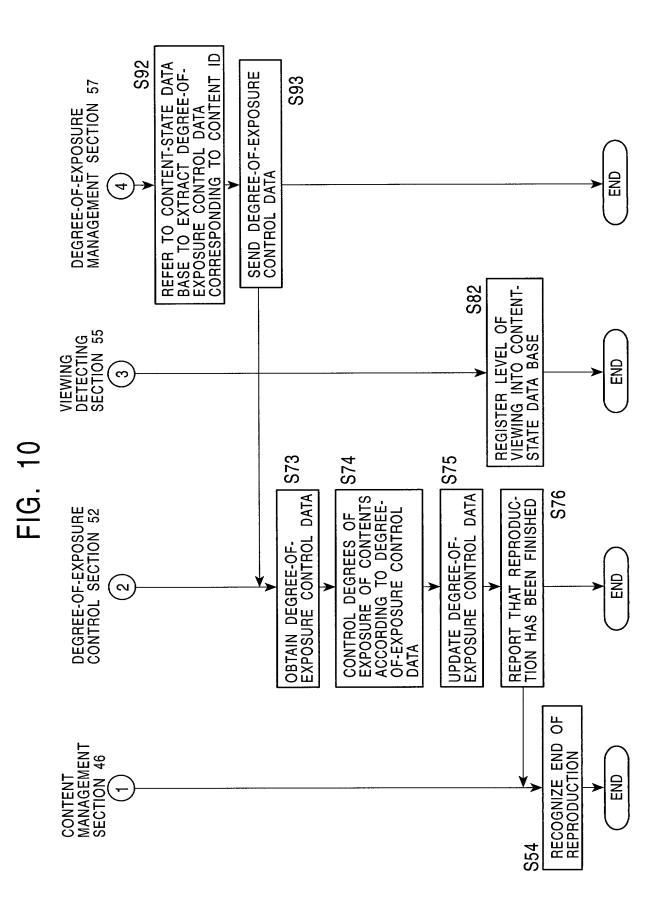
FIG. 5B



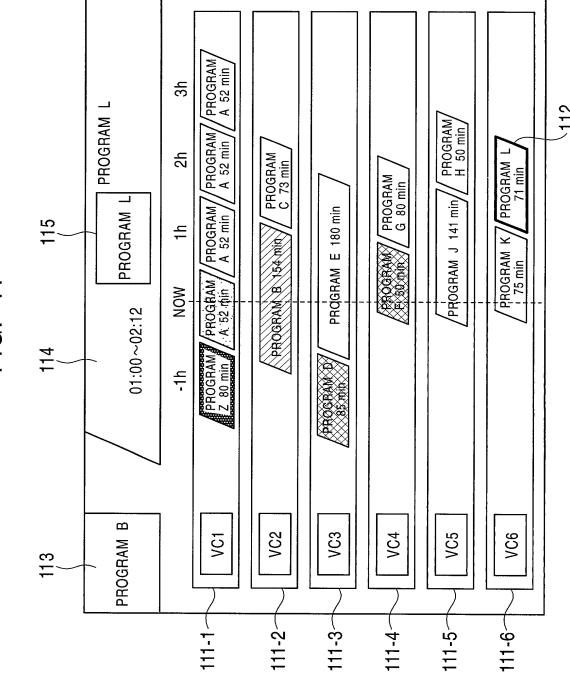








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